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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,684	07/20/2001	Michael Y.T. Hwang	018170002600	2529

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EXAMINER	
VO, TUNG T	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/910,684	HWANG ET AL.	
	Examiner	Art Unit	
	Tung T. Vo	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 9-10, 12-14, 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Anesko et al. (US 5,987,178).

Re claims 1 and 12, Anesko discloses a method for loading pixels into a temporary memory (51 of fig. 8) comprising:

loading a block of pixels into said temporary memory (MEMEM, 51 of fig. 8, e.g. the DMA BUS, 32b, is loaded to a 8 bank memory);

loading a staging memory (55 of fig. 8) with pixels for updating said block of pixels (60 of fig. 8, e.g. a memory address generator is generating the 8 bank memory for updating),

an address translator (64 of fig. 8, e.g. rotate array of pixels means rearranges locations of pixels) rearranging said pixels so that an update group of pixels can be accessed in parallel from said staging memory (col. 4, lines 42-48, e.g. the memory and PE array provide a pipelining mechanism that provides the ability to rotate the reference block within the array while it is running, and simultaneously read the memory contents into the array using a dual addressing mechanism; see also col. 7, lines 21-32);

and address unit (60 of fig. 8, e.g. memory address generator) updating said block of pixels in said temporary memory with an update group of pixels from said staging memory in parallel (col. 7, lines 11-20, fig. 13).

Re claims 2 and 17, Anesko further discloses wherein said temporary memory (51 of fig. 8) is connected to a processing unit (52 of fig. 8) for comparing said block of pixels to a second block of pixels (col. 7, lines 11-40).

Re claims 3 and 16, Anesko further discloses wherein said temporary memory is a two-dimensional shift register (figs. 4 and 5), and wherein said update group of pixels corresponds to a shifted row or column of said block of data (figs. 3 and 5).

Re claims 4 and 18, Anesko further discloses wherein said processing unit performs a comparison for a motion estimation algorithm (col. 7, lines 20-32).

Re claims 5 and 14, Anesko further disclose wherein said staging memory (55 of fig. 8) comprises banks of memories (8 banks of staging memory 55 as shown in fig. 8), each bank providing a different one of said update group of pixels (col. 7, lines 50-57).

Re claim 6, Anesko further discloses wherein said update group of pixels is a row or column (fig. 10, e.g. columns stripes).

Re claim 7, Anesko further disclose a search pattern that can be executed by loading said temporary memory, in a single cycle, with pixels to provide a next block to be searched (col. 7, lines 11-20; and col. 9, lines 7-26).

Re claims 9 and 13, Anesko further discloses wherein said rearranging of said pixels comprises reordering said pixels in each row so that each pixels from a single column are spread across a plurality of columns so that they can be accessed in parallel (col. 4, lines 42-48, e.g. the memory and PE array provide a pipelining mechanism that provides the ability to rotate the reference block within the array while it is running, and simultaneously read the memory contents into the array using a dual addressing mechanism; see also col. 7, lines 21-32).

Re claims 10, Anesko further discloses a method for loading pixels into a temporary memory (51 of fig. 8), comprising:

loading a block of pixels into said temporary memory, said temporary memory being a two-dimensional shift register (DMA BUS, 32b of fig. 8);

loading a plurality of memory banks (8 BANKS MEMORY, 55 of fig. 8) with pixels for updating said block of pixels in said two-dimensional shift register, by rearranging said pixels so that a column or row of pixels can be accessed in parallel from said memory banks (64 of fig. 8, e.g. rotating pixels);

executing a search pattern wherein each block in said search pattern differs from a previous block by a single row or column (52 of fig. 8); and

updating said block of pixels in said temporary memory with a new row or column from said memory banks in parallel (60 of fig. 8, e.g. addressing the new pixels in row or column).

Re claim 19, Anesko discloses an apparatus comprising:

a two dimensional shift register for storing a block of pixels (51 of fig. 8);

a processing unit (52 of fig. 8) coupled to said two dimensional shift register, said processing unit being configured to simultaneously compare each pixel in said block of pixels with a reference block of pixels;

a plurality of memory banks (55 of fig. 8) for storing new pixels for updating said block of pixels;

an address translator (64 of fig. 8) coupled to an input to said plurality of memory banks for rearranging said new pixels so that an update group of said new pixels can be accessed in parallel from said plurality of memory banks;

an addressing unit (60 and 64 of fig. 8) for reordering a group of pixels accessed in parallel from said plurality of memory banks to said two dimensional shift register, correcting for rearrangements made by said address translator to allow said new pixels to be accessed in parallel.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anesko et al. (US 5,987,178) as applied to claims 1 and 10, and further in view of Andrew et al. (US 5,428,403).

Re claims 8 and 11, Anesko teaches the full search technique for motion estimation (col. 7 and 8) except the search pattern is a spiral search pattern as claimed.

However, Andrew teaches the search pattern is a spiral search pattern that is used for motion estimating (fig. 4). Therefore, taking the combined teachings of Anesko and Andrew as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Andrew into the apparatus of Anesko for performing the spiral search pattern. Doing so would improve a quality of encoded image as suggested by Andrew (col. 12, lines 40-47).

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anesko et al. (US 5,987,178) as applied to claim 12, and further in view of Kalapathy (US 5,799,169).

Re claim 15, Anesko teaches the staging memory (55 of fig. 8) but Anesko does not particularly disclose the staging memory comprises SRAM memory as claimed.

However, Kalapathy teaches a SRAM memory is used in the motion estimation (111 of fig. 1). Therefore, taking the teachings of Anesko and Kalapathy as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the SRAM (111 of fig. 1) of Kalapathy into the motion estimator of Anesko for the same purpose to storing the new pixels to be updated. Doing so would allow the CPU to indicate that immediate processing of the queued instructions is advantageous in order to avoid unnecessary stalls.

6. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anesko et al. (US 5,987,178) as applied to claim 19, and further in view of Maturi et al (US 5,731,850).

Re claim 20, Anesko teaches the search left to right and top to bottom as shown in column 9, +/-1 search pattern but Anesko does not particularly four buffers coupled to said two dimensional shift register for buffering new rows and columns of pixels to be shifted in from the left, right, top and bottom as claimed.

However, Maturi teaches four buffers coupled to said two dimensional shift register for buffering new rows and columns of pixels to be shifted in from the left, right, top and bottom (col. 9, lines 30-67, e.g. 4 registers store the f.sub.-- codes used to determine the motion estimation search ranges for B-frames which are located 2, 3 or 4 frames). Therefore, taking the combined teachings of Anesko and Maturi as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Maturi into the motion estimator of Anesko for the same purpose of performing the left, right, top, and bottom search. Doing would take advantage of the high-resolution capability of a hierarchical block matching motion estimation.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takano (US 6,212,231 B1) discloses an assign of pels a macroblock for compression encoding to a memory sequence in one of banks of DRAM.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung T. Vo whose telephone number is (703) 308-5874. The examiner can normally be reached on 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris. Kelley can be reached on (703) 305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TUNG T. VO
PATENT EXAMINER

Tung T. Vo
Examiner
Art Unit 2613

T.Vo